Designer's Guide Consulting
Analog Verification

ANALOG VERIFICATION NEWSLETTER

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Contents

Greetings

Dear Friends and Colleagues,

Our newsletter is back! Much has happened since we started Designer's Guide. In 2005, Analog Verification (AV) was a nascent idea. Three years later, in 2008, companies began to implement AV. Today, in 2011, companies who went down this path are focused on seeing how they can make AV more efficient and cost effective as they attempt to scale AV company-wide. There are also many companies, who are just beginning down the path of AV as their chips reach a stage of complexity where they are seeing bugs in the analog, the analog-digital interface, and the RTL and embedded software that talks to the analog.

To read about what Designer's Guide is doing to help with AV adoption and proliferation, please see the article entitled, "What's New at Designer's Guide." We're also announcing our AV training schedule for 2011. Please see the section, "4 Day Training Class: Analog Verification."

Finally, our main newsletter article is entitled, "Considerations When Starting Analog Verification." We present our experiences and suggestions when embarking on AV for the first time.

We would also like remind everyone that the main focus of our company is to offer services and now also solutions to help your company transition to analog verification. Details on our services can be found at *www.designers-guide.com/services*. Please contact us directly if you are interested in our solutions.

As always, feedback is greatly appreciated.

Sincerely,

Henry Chang and *Ken Kundert*

4 Day Training Class: Analog Verification

2011 Schedule

- 16 May — 19 May, 2011 in Mountain View, California
- 13 September — 16 September, 2011 in Mountain View, California
- 6 December — 9 December, 2011 in Mountain View, California

This challenging four day course provides participants with the tools they need to take on the task of verifying complex analog, RF, and mixed-signal integrated circuits. It combines lecture

with a substantial amount of time in the lab to teach the overall analog verification process. You will learn how to develop a verification plan, functional models of analog blocks, regression tests for those models, and a fully verified Verilog model for the entire analog portion of the design for use in chip-level verification. New to the class will be material on how to accomplish AV more efficiently. Besides offering open classes, our classes are also available to be taught on-site at companies throughout the world. Please contact us if interested.

Target Audience. The target audience for this class is for those who anticipate practicing AV, those who want to improve their AV skills, or those who want an in depth, hands-on feel for what AV is. We spend considerable time discussing the common mistakes people make when using Verilog-AMS and how to avoid them, so the class is also very appropriate for those interested in learning or improving their skills with Verilog-AMS. These target audience includes: analog verification engineers, analog designers, analog design leads, and digital verification engineers and CAD engineers.

Instructors. Ken Kundert and Henry Chang.

Prerequisites. Students should have a working knowledge of Verilog-A, analog circuits, and the Cadence design environment. It is also helpful to have gone through Verilog-AMS training. The better prepared you are, the more you will get from the class.

Cost. $2650 per attendee.

For more information or to sign up, visit *www.designers-guide.com/classes*. Space is limited, so please contact us without delay to reserve a spot.

What's New at Designer's Guide

Designer's Guide is a company dedicated to Analog Verification (AV). In 2005, we focused on explaining the needs and benefits of AV, and worked with companies on design projects to test AV ideas — all the while finding bugs. In 2008, as companies began to implement AV, we began AV training classes — on site and open to the public. We continued to provide consulting, modeling and regression test writing services to help companies succeed at AV. Now, in 2011, we're in a new phase. Even as early as 2008, we recognized that there are key limiting factors in AV adoption — none of which are in the idea or methodology, but all in the efficiency, training, and cost effectiveness of implementing AV. It was then that we began to develop solutions to address these issues of sustainability and scalability while at the same time improving the AV methodology. We'll discuss these solutions in future newsletters. However, if you are interested now, please don't hesitate to contact us. We have presentations, brochures, and video demonstrations available.

We also just added a global sales force. To find a sales representative near you, please visit *www.designers-guide.com/contacts*.

Considerations When Starting Analog Verification

By Henry Chang and Ken Kundert

We've helped and talked to many companies interested in adopting Analog Verification (AV). In this article, we present a list of considerations and hope to correct some common AV misconceptions. We offer an assessment service, where we look at what you're trying to accomplish, the types of designs you're working on, your levels of staffing, and make recommendations to get you off to a good start on AV. However, if you're more of a do-it-yourself kind of company, here are our general recommendations.

Again and again, we see that the companies that are the most successful in getting started with AV and in making it sustainable are those that get buy-in from all of the key players — the management, the chip-lead, the analog designers, and the CAD group. The management has to believe that an investment in AV is worth it, i.e. investing time, money, and effort to catching functional bugs in the analog, the analog-digital interface, and the RTL and embedded software that talks to the analog is worth the extra cost for potentially saving a tape-out, or for the often priceless ability to get first functional silicon to their end customer *on time* and in a *repeatable* manner.

The second key player is the chip-lead. If AV is going to be applied, the chip-lead must be on board with the idea. Usually, the chip-lead is the easiest person to convince. Our rule of thumb is that typically unless you're seeing many functional bugs, AV is not necessary until there are at least four or five designers working on a chip. This is when the chip-lead's job becomes particularly challenging. While the block designers are focused on designing the analog blocks, the RTL, and even the embedded software, the chip-lead is in charge of stitching it all together. This includes writing the chip-level documentation, putting together the top-level schematics, designing the overall chip architecture, watching the design of all of the blocks, and following-up with all of the engineers as needed. The chip lead's job may also include working with the end customer and working with the people in charge of the downstream process of getting the tape out data into manufacturing. And finally, the chip-lead is in charge of making sure all of this is done correctly. While the designers usually have their blocks under control, the chip-lead is often stretched thin. Usually, the chip-lead has no time for any kind of AV effort even though part of the chip-lead's job is to make sure the chip is functional. We were once told by a chip-lead, that "leading" is not what characterizes his job. It's always being behind. As long as management is willing to invest in AV, AV is really there to solve one of the open challenges the chip-lead has — finding all of the bugs on the chip.

Analog block designers often see the benefit of AV. They understand that their blocks both need to meet functional and performance specifications. However, we've run across skepticism from analog block designers for two reasons. First, an analog designer's blocks may be functionally simple enough that no functional problems have ever arisen. Most do, however, understand that even if functionally simple, their blocks still need to talk to the rest of the chip and that this must be verified. Second, for most analog blocks, meeting performance specifications represents the primary challenge in their design. In this sense, AV doesn't address their problem directly. AV can help, but usually only a little. Another reason for reluctance on the part of the analog designer for AV is the misconception that AV is going to take a lot of their time. When we deploy AV, our goal, is to minimally disrupt the design process, and part of that is to take as little time away from the analog designers as possible. Once even the skeptical ones understand this, they usually go along with it. And if not, they are finally convinced when the management tells them that they are bringing on additional people for the AV effort.

Now as it turns out, even the skeptical analog designers by the end of the project, are strong supporters of AV. They come to learn the benefits of AV with respect to their blocks. The benefits include knowing that their block is being used correctly in the overall chip. Part of AV includes running a lot of simulations on their blocks, and we do find functional issues. And as much as analog designer don't want to be bothered, having another pair of eyes looking at their blocks has often proved valuable even when evaluating performance. Even if it's not the focus of AV, often, another engineer can point out something that can be improved or raise potential issues on the design. This is especially true with an AV engineer as this other pair of eyes becomes very knowledgeable about the analog designer's transistor level design, because the AV engineer is simulating it. Finally, part of AV is to develop functional models for the analog blocks. Having

models that the analog designers didn't have to write and that are verified to be functionally equivalent to schematics saves the analog designers time in that they don't have to write their own models.

Finally, the CAD group needs to be convinced. Usually, this isn't very difficult also. The CAD group usually has an eye toward improving methodology, and this gives them an opportunity to participate in potentially greatly improving the chances for first functional silicon. Their support is, of course, needed to make sure that the correct tools are in place for AV, and to support any issues that arise. Often times AV exercises a tool flow that is new to a company, and lots of little issues need to be resolved. Fortunately, there are almost always known solution to the issues. It's just a matter of uncovering them and resolving them one by one.

One caveat is that although we stand by our comment about taking as little time from the analog designers as possible, there is management debate as to what is the best approach — having analog designers do the AV, having *dedicated* analog verification engineers do the AV, or having a blend. At present, our experience is that with what's available in terms of tools, methodologies, training, analog verification IP, it's not possible for the analog designers to do the AV alone. A blend may be possible, and certainly we've had success when there are dedicated AV engineers. Since it is such a strong desire for many companies to get the analog designers involved, as Designer's Guide develops solutions that make overall gains in reducing the cost of AV and in improving AV coverage, we are also looking toward making it possible for analog designers to *naturally* get involved by delivering them value with minimal effort and leveraging a task that they already do in a way not done before. Please contact us, if you'd like more details.

Suppose now that all of these groups are in agreement that AV should be tried. Certainly, our recommendation is that you start by deploying AV on only one or two projects. It probably goes without saying to not try to do this company wide initially, but we'll mention that the experience you'll gain from doing a few trial projects with AV will significantly help you in figuring out the best way to deploy AV company wide.

In getting started, we first recommend that you learn as much about AV as you can. This will save a lot of time and headache in the long run. We can help you with this, or seek out other AV experts. Learning includes:

- Reading any literature available on the topic. Understand the scope of the problem, and understand the entire AV process from planning, to writing the models and testbenches, to AV signoff.
- Having us do an assessment and provide recommendations. We've helped transition companies to AV many times, and as much as each company believes they are unique, there are usually more similarities than differences, and we can leverage our experience to make deploying AV easier. We believe that the reason why companies are more similar than different is that the need for AV isn't so much from a particular style of design that a company employs, but in how their design engineers communicate or fail to communicate with each other. There seem to be a lot of similarities in the way engineers communicate. For example, the state of design documentation seems to be a universal constant across most companies.
- Having the people who will be doing AV take a class on AV. There's more to AV than just writing models, and even with writing models, there's a big difference between writing good AV models and testbenches and writing good Verilog-A models. The focus of AV models and testbenches is to play a role in being effective and efficient in the overall AV process.
- If possible, having people who have AV experience work or consult on the project. Just like in any engineering discipline, experience will make all the difference in success versus failure.

The skills required for AV cannot be picked up overnight. A class on AV will give an engineer a good start, but experience still counts!

When setting up AV, we suggest keeping the following in mind:

- Set up the project in such a way as to minimally impact the design process. Doing AV certainly should not delay the tape-out process. This will likely mean making sure that adequate resources are deployed on AV.
- AV should begin at the start of the project, not in the middle or end. Unfortunately, little benefit comes from doing AV as an after thought. A critical aspect to AV and from where a significant amount of its benefits is derived is when chip-level simulations are run. To get to this stage, a significant amount of AV work needs to be accomplished. AV is one of those methodologies where the majority of the work has to be done *before* the majority of the benefits are accrued. For example, it could be that the first 80% of the work only yields 20% of the benefits. It's not until that first 80% is done, that one sees the remainder of the benefits. AV is an "all-in" process. You either do it, or you don't. Doing a partial job will likely be waste of time.
- Even though it's been said before, it's worth repeating. AV is not about catching performance issues, it's about catching functional problems. While it is possible to use the tools and techniques of AV to help with performance verification in some important cases, if you try to use models to access performance across the board you will likely increase the amount of effort you need to expend by a factor of five!
- AV is a methodology. There is a science and process to it. Getting only modeling expertise is not sufficient. There's AV planning, understanding coverage, being able to write AV testbenches, and most importantly, making a seemingly unbounded effort bounded.
- Deploy dedicated resources to AV. It doesn't have to necessarily be an AV engineer, but it does need to be someone dedicated. There are a lot of analog designers who, with some training, would be great at AV. If they have interest, they could easily be that dedicated resource, but they have to be dedicated. Tape-out is always the primary concern, and more often than not, it's at risk of slipping. If the decision is not made to dedicate AV resources, anyone working on it will likely be diverted to design, and AV will not be done. In fact, we have never seen AV work without dedicated AV resources. The analog designers can certainly be involved, and, in future, with our solutions, they may be significantly involved, but someone needs to be dedicated so that steady progress is made with respect to AV.

Finally, recognize that AV will be difficult the first time through (and probably the second). We've gone though many initial AV efforts with many companies. We always find bugs, but it's a lot of work, and there are always surprises the first couple of times through, so don't use the initial cost spent to guide the decision as to whether or not to do it again. Focus on using the initial project on understanding what AV is capable of, and deciding whether or not it makes sense to deploy AV on other projects. Expect that the cost of AV will go down as you gain more experience with AV. In the initial project, a new AV engineer could be 3× to 10× slower than an experienced AV engineer. Also, there is no reuse of models and testbenches from previous designs. Significant productivity gains will be achieved with more experienced AV engineers and reuse.

A good propagation strategy is to start with a foundational product (one that is expected to be the basis for several follow-on products). Expect that the initial use of AV will be slow and expensive as you build up expertise and a repository of models and testbenches. From this initial project, you can then expand the use of AV to other designs in the same product line, and begin the use of AV on foundational products in other product lines. As you apply AV on the follow-on designs, you'll discover that AV will be considerably cheaper and more effective.

In future newsletters, we will be discussing solutions which will reduce cost in each of the phases of the adoption of AV from initial to full company-wide deployment.

We wish you luck on this, and please don't hesitate to contact us for any assistance.