



Contents

- 2 - Announcements
- 2 - Designer's Guide Web Resources

Greetings

Dear friends and colleagues,

Welcome to the first issue of our Analog Verification newsletter. Analog verification represents a critical evolution in the way analog, mixed-signal, and RF chips are designed. Analog verification is the separate and systematic process of verifying an analog, mixed-signal, or RF design. The first and foremost goal is to verify that what is implemented in transistors functionally matches the specifications and any models created. From there, performance specifications are verified as dictated by the verification plan that is written as part of the process. The sole purpose of analog verification is to look for errors and is performed as a step distinct from the design process. As complexity grows in analog designs, companies are now adopting analog verification as companies did with digital verification a decade ago.

It has been over two years since we started Designer's Guide Consulting to help bring analog verification to semiconductor and fabless semiconductor companies. Along the way, many ideas, tips, questions, and issues have arisen. Each month, we will pick up one of these relevant topics and discuss it. We have many future articles planned. These include how performance verification is addressed, what types of designs are most suited to this approach, what the skill set requirements are for an analog verification engineer and how many are needed given a particular design, what tools are required, practical approaches to transitioning to analog verification, and how analog verification can be a natural stepping stone to top-down design. Starting with the next issue, we will have a web page where you can comment on our articles. We'll also include relevant announcements. In this newsletter, we will talk about web resources for analog verification and in particular, the two Designer's Guide websites. Our first announcement is that Ken will be giving his popular cyclostationary noise talk at three free Agilent hosted seminars (details below). From time-to-time, we'll also discuss other topics that we hope you will find interesting.

The mailing list program we're using allows you to subscribe or unsubscribe to our lists. By default, you are subscribed. We envision the frequency of messages will be very low (i.e. one to two messages per month). We hope that you will continue to subscribe to these mailings. We will strive to keep the mailings relevant and succinct. If there are topics you'd like us to discuss or you have any comments, please mail them to consulting@designers-guide.com. We apologize if you receive multiple copies of this newsletter or if this topic is of no interest to you. If you do not want to receive this mailing, please follow the instructions below to unsubscribe. For any issues, please contact consulting@designers-guide.com.

Sincerely,

Ken Kundert, President, Designer's Guide Consulting, Inc.

Henry Chang, Vice President, Designer's Guide Consulting, Inc.

Announcements

Ken to Present at Agilent RFIC Seminar

Ken will be giving one of his signature talks, "Noise in Mixers, Oscillators, Samplers, and Logic - An Introduction to Cyclostationary Noise" at the Agilent EEs of RFIC Seminar, "Tackling the Tough Problems." This is a free half day seminar that will provide insight and practical design methodology suggestions for achieving a higher likelihood of first time success for RFIC designs.

The seminar features three other speakers who will focus on RF transceiver design. They will provide a practical overview of solutions addressing the key design challenges of RFICs: noise; design for yield; complex modulated signals and their interaction on chip; and how to handle large highly integrated design characterization even with fully extracted parasitics. The seminar is intended for RFIC designers (cellular transceivers, WLAN, WiMAX, Power Amps, etc.), RFIC design managers, CAD engineers supporting RFIC designers, CAD managers, and all those involved in the design, verification and characterization of RFICs.

The seminar is free and lunch will be provided. The dates/times for these seminars are listed below:

- July 24, San Diego, CA, Four Points Hotel, 10am-3pm
- July 25, Irvine, CA, Hilton, Irvine/Orange County Airport, 10am-3pm
- July 26, Santa Clara, CA, Agilent Technologies, 10am-3pm

If you are interested, please visit eesof.tm.agilent.com/news/news400.html#rfic_seminar.

Designer's Guide Web Resources

In this first issue, we will describe the two websites we have. The first is the Designer's Guide Community website (www.designers-guide.org). This is a website that encourages the sharing of questions and information from the entire analog, mixed-signal, and RF design community and those that support it. The website contains a wealth of information including papers on design, analyses, and modeling. There are links to the best books on analog design and Verilog-A/MS modeling examples. By far the most popular feature of this website is the Forum where over 4500 registered members add over 10 posts per day. You might be interested to know that we have 500 to 600 visitors per day visiting the website. We think this is a very respectable number given the size of the community. We are in the process of adding new features to make this community website even more vibrant. We encourage you to visit the web site. There is no charge for using it.

Our second website is the Designer's Guide Consulting website (www.designers-guide.com). This website is dedicated to our consulting business. This website describes the basics of analog verification. We've also posted papers we've written on this topic. Finally, it describes the services we offer such as the lectures, training, and consulting to help companies transition to analog verification. We're also working on improving this web site. Eventually, this is where you'll be able to comment on these newsletters

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