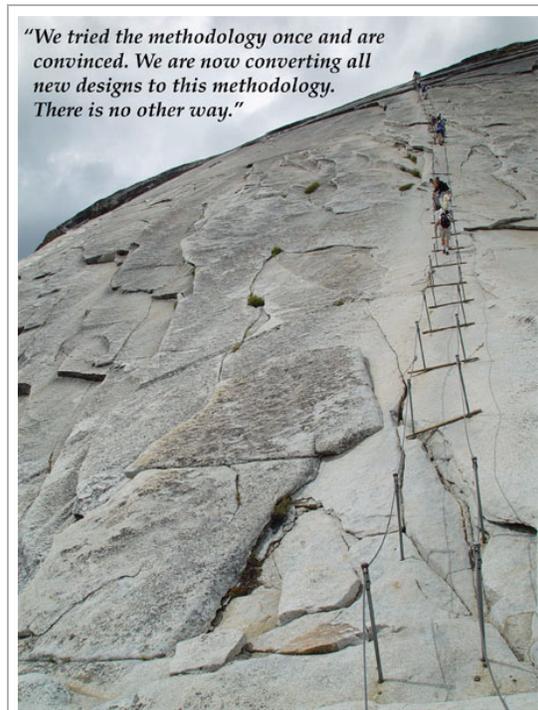# Analog Verification

ANALOG DESIGNS HAVE CHANGED. Whereas we used to design opamps, we now design multimode wireless transceivers. And while the scale of the designs has obviously grown fantastically, the character of the designs have changed just as much. Analog designs have hundreds of modes and thousands of settings. They implement sophisticated algorithms and contain blocks that are self calibrating and self adapting. In a word, they are complex. And while it is their performance that commands most of the attention of the people that design them, it is now their complexity that is the source of most of the catastrophic failures in their design. While this is a new situation for analog circuits, it has been true for digital circuits for many years. Digital design teams addressed this problem by adopting a strong functional verification methodology driven by verification engineers. Analog designs have now gotten to the point where analog design teams must do the same.

"We can no longer live with the respins. We need a better way."

TRANSISTOR-LEVEL SIMULATION IS TOO SLOW. Analog designers have traditionally relied on transistor-level circuit simulation to verify their circuits. However, today's designs are so large that it may take several weeks to simulate a single aspect of a complete circuit. With a circuit that has multiple behavioral modes, each must be checked individually in order to expose all of the functional errors in the design. For a design that implements hundreds of modes and thousands of settings, this may require many years, and perhaps decades, of simulation time. Switching to the so called "FastSPICE" simulators, which are faster but less accurate and less reliable, can provide some relief, but they are still orders of magnitude too slow to be able to completely verify all modes and settings of a complex analog design.

"We tried the methodology once and are convinced. We are now converting all new designs to this methodology. There is no other way."

A NEW APPROACH IS NEEDED. Designer's Guide Consulting is a unique consulting firm that specializes in helping companies transform their design process to one that employs a rigorous analog verification methodology. This methodology is much like the one used by digital verification groups. Once adopted, design teams are typically able to fully verify

the functionality of their designs to the transistor level every night using pass/fail regression tests. Not only does this methodology fully verify the design, but it also produces a fully verified high-level Verilog model of the design and confirms that both the design and the model are consistent with the stated functional specifications. And while the primary concern of the methodology is functional verification, it also supports performance verification by dramatically accelerating the simulation of non-critical blocks.

A PROVEN METHODOLOGY. The methodology taught by Designer's Guide Consulting has been used with great success by a handful of companies and was recently applied to the analog portion of a large mixed-signal SoC. The verification process entered its final phase during tape out. At this point the designers believed the design to be complete and ready to go. However, a half dozen functional errors were hiding in the design, all of which were exposed using the methodology. These errors were all centered around the part of the circuit that had the most difficult performance requirements and was the most difficult to simulate. The design team was so focused on meeting the performance requirements that they never got around to verifying the basic functional requirements; a very common source of errors. In another case the errors were hiding in the digital cir-

cuitry that processed the signals produced by the analog section. Here the fully verified Verilog model of the analog section allowed the digital RTL code to be tested with the analog portion of the design, which exposed these errors.

THE RACE GOES TO THE SWIFT. While this is a proven methodology that has shown itself to be both efficient and effective, it is not in widespread use at this point. Conditions are only now getting to the point where its use is becoming essential. Adoption is slowed by the fact that it

"*A systematic analog verification methodology is a huge differentiator in the design of today's complex consumer electronic ICs.*"

requires new skills in the design teams and because its importance is not yet recognized. Eventually everyone designing complex chips that involve analog will use this methodology. Nevertheless the current situation represents an important advantage to those that have mastered the methodology as it represents a substantial differentiator that could last for years.

FIND OUT MORE. You can find out more about this methodology by reading the papers found on the *Documents* page of our website, *www.designers-guide.com.* There are a variety of ways that we can help you get started: including a simple introductory presentation, an evaluation of your current methodology, training, and methodology transformation services. If this methodology sounds interesting to you, please give us a call.

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